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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,608	03/10/2004	John Turner	015114-070400US	6189

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TOWNSEND AND TOWNSEND AND CREW LLP/ 015114
TWO EMBARCADERO CENTER
8TH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
AUDUONG, GENE NGHIA	
ART UNIT	**PAPER NUMBER**
2827	

DATE MAILED: 12/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/798,608	TURNER, JOHN	
	Examiner	Art Unit	
	Gene N. Auduong	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-37 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-37 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 8-30-04; 9-30-05.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement (IDS) submitted on August 30, 2004 and September 30, 2005 is being considered by the examiner.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-37 are rejected under 35 U.S.C. 102(b) as being anticipated by Wahlstrom (US Pat. No. 6,335,896).

Claims 12-37 are rejected under 35 U.S.C. 102(b) as being anticipated by Sasaki (US Pat. No. 4,768,172).

Regarding claim 1, Wahlstrom discloses an integrated circuit comprising an array of DRAM cells as in figure 15, each DRAM cell comprising: a first transistor having a gate coupled to a read word line WLR and a drain coupled to a read bit line BLR; a second transistor coupled in series between the first transistor and a power supply voltage Vss; and a third transistor coupled between the gate of the second transistor and a write bit line BLW, a gate of the third transistor being coupled to a write word line WLW, wherein the write word line WLW is not directly connected to the read word line RW (figure 15; col. 2, lines 65+).

Regarding claim 2, Wahlstrom discloses the integrated circuit according to claim 1 wherein the integrated circuit is a field programmable gate array, and the gate of the second

transistor is coupled to a pass gate in the field programmable gate array (gate of second transistor coupled to the control node, which is to the gate of other controlled transistor as in figure 13F).

Regarding claim 3. The integrated circuit according to claim 2 wherein the pass gate is a programmable routing connector that couples interconnect lines on the field programmable gate array (figures 13F and 15).

Regarding claim 4, Wahlstrom discloses the integrated circuit according to claim 2 wherein the pass gate is used to configure logic performed by logic circuitry on the field programmable gate array (to control the function of the cell).

Regarding claim 5, Wahlstrom discloses the integrated circuit according to claim 1 further comprising: a capacitor coupled to a gate of the second transistor (figure 15).

Regarding claim 6, Wahlstrom discloses the integrated circuit according to claim 5 wherein the capacitor is a planar capacitor or a trench capacitor (figure 2a, 15 and its description).

Regarding claim 7, Wahlstrom discloses the integrated circuit according to claim 5 wherein the capacitor is a quasi-static DRAM capacitor fabricated with nano-crystal oxide (not specifically disclose the type of dram, but the memory device can be used any known cell type).

Regarding claim 8, Wahlstrom discloses the integrated circuit according to claim 1 further comprising: a CMOS inverter having an input coupled to the gate of the second transistor, wherein the integrated circuit is a programmable integrated circuit, and an output of the CMOS inverter drives a pass gate that programmably couples interconnect lines on the programmable integrated circuit (figures 8B and its description).

Regarding claim 9, Wahlstrom discloses the integrated circuit according to claim 8 wherein the third transistor is a p-channel field effect transistor, and the input of the CMOS inverter is not directly connected to an N-type doped semiconductor region (figures 8A-8B).

Regarding claim 10, Wahlstrom discloses the integrated circuit according to claim 1 further comprising: a sense amplifier having an input coupled to the read bit line; a multiplexer having a first input coupled to an output of the sense amplifier; and a driver coupled between an output of the multiplexer and the write bit line (figure 1).

Regarding claim 11, Wahlstrom discloses the integrated circuit according to claim 10 further comprising: a data shift register coupled to a second input of the multiplexer; an error detection circuit coupled to an output of the data shift register, the error detection circuit performing error detection on data stored in the DRAM cells (Col. 2, lines 65+).

Regarding claim 12, Sasaki discloses an integrated circuit comprising an array of DRAM cells, each DRAM cell as in figures 4-6 comprising: a first transistor 29 having a gate coupled to a read word line WL2 and a drain coupled to a read bit line BL2; an inverter 5 having an output coupled to a source of the first transistor 29; and a second transistor 27 coupled between an input of the inverter 5 and a write bit line BL1, a gate of the second transistor 27 being coupled to a write word lineWL1 (figure 4, 3, lines 33+).

Claims 13-18 contain the similar limitation as previously discussed in claims 2-11. Therefore, they are analyzed as previously discussed with respect to claims 2-11.

Regarding claims 19-32, the apparatus as previously discussed in claims 1-11 and 12-18 would be performed the method as claimed. Therefore, they are analyzed as previously discussed with respect to apparatus claims 1-11 and 12-18.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gene N. Auduong whose telephone number is (571) 272-1773. The examiner can normally be reached on 9-5-4, alternate second Monday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GA
November 30, 2005

Gene N Auduong
Primary Examiner
Art Unit 2827